PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	)
	)
Singh et al.	) Art Unit: 2811
	)
Application No. 10/633,004	) Examiner: Vu, Hung K
	)
Filed: 07/31/2003	) Date: January 30, 2007
	)
For: PAD OVER ACTIVE CIRCUIT SYSTEM AND METHOD WITH MESHED SUPPORT STRUCTURE	)
	)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ATTENTION: Board of Patent Appeals and Interferences

REPLY BRIEF (37 C.F.R. § 41.37)

This Reply Brief is being filed within two (2) months of the mailing of the Examiner's Answer mailed on 11/30/2006.

Following is an issue-by-issue reply to the Examiner's Answer.

II RELATED APPEALS AND INTERFERENCES (37 C.F.R. §41.37(c)(1)(ii))

With respect to other prior or pending appeals, interferences, or related judicial proceedings that may directly affect, or be directly affected by, or have a bearing on the Board's decision in the pending appeal, an appeal noted on 06/20/2006 in application serial number 10/633,021, an appeal noted on 06/19/2006 in application serial number 11/067,551, and an appeal noted on 12/1/2006 in application serial number 11/046,420 may be, but are not necessarily, related.

Since no decision(s) has been rendered in such proceeding(s), no Related Proceedings Appendix is appended hereto.

VII ARGUMENT (37 C.F.R. § 41.37(c)(1)(vii))

Issue #1:

The Examiner has rejected Claims 1-2, 4-18, 20-21, 27, and 29-30 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

Specifically, the Examiner has argued that the specification does not disclose an entirety of at least one of the transistors being disposed directly below the bond pad, as recited in Claim 1, 20 and 21. On page 3, lines 10-11 of the originally filed application, it is disclosed that "the active circuit may include a plurality of transistors." Further, Claim 21 of the originally filed application discloses "a plurality of transistors forming a core of circuits." Still yet, on page of 7, lines 16-17 of the originally filed application, it is disclosed that "the bond pads 306 may be disposed above the core 302, and/or any other part of the active circuit 308." By virtue of this and other disclosure, appellant's claims clearly meet the written description requirement.

In the Examiner's Answer mailed 11/30/2006, the Examiner has argued that "it is disclosed that the active circuit may include a plurality of transistors" and that "a plurality of transistors forming a core of circuits" is also disclosed. The Examiner has further argued that "it is disclosed [that] the bond pads 306 may be disposed above the core 302, and/or any other part of the active circuit 308," but that "there is nothing in the instant application [that] discloses an entirety of at least one of the

transistors being disposed directly below the bond pad." The Examiner has also argued that "the bond pad 306 may be disposed above the core 302, and/or any other part of the active circuit and the active circuit may include a plurality of transistors, but it does not necessarily mean an entirety of at least one of the transistors being disposed directly below the bond pad."

Appellant respectfully disagrees. As shown in the exemplary embodiment of Figure 3, a plurality of bond pads (item 306) are depicted to be directly above the I/O bus (item 304) of the active circuit (item 308). Further, on page 3, lines 10-11 of the originally filed application, it is disclosed that "the active circuit may include a plurality of transistors." In addition, on page 7, lines 13-17, it is disclosed that "the bond pads 306 may be disposed above the core 302, and/or any other part of the active circuit 308" (emphasis added). Thus, the following disclosures are made:

1) a plurality of bond pads (item 306) are shown in the figures to be *directly* above the I/O bus (item 304) of the active circuit (item 308), in accordance with one embodiment disclosed in the figures;
2) another embodiment is disclosed in the specification where the bond pads (item 306) may be disposed above the core (item 302) AND any other part of the active circuit (item 308); and
3) the core (item 302) of the active circuit (item 308) includes a plurality of transistors.

Therefore, appellant respectfully asserts that the specification, as originally filed, does indeed *explicitly* disclose appellant's claimed "entirety of at least one of the transistors is disposed directly below the bond pad," as claimed.

Even assuming *arguendo* that somehow the original disclosure does not *explicitly* disclose the claimed "entirety of at least one of the transistors ...[being] disposed directly below the bond pad," such disclosure is clearly *inherent* in view of disclosures 1)-3) noted above.

The Examiner is reminded that, by disclosing in a patent application a device that inherently has a property, a patent application necessarily discloses that property, even though it says nothing explicit concerning it. The application may later be amended to recite such item without introducing

prohibited new matter. *In re Reynolds*, 443 F.2d 384, 170 USPQ 94 (CCPA 1971); In re Smythe, 480 F. 2d 1376, 178 USPQ 279 (CCPA 1973). See also MPEP 2163.07(a).

Of course, it should be noted that such citations are set forth by way of example only and should not be construed as limiting to the claims in any manner.

Issue # 2:

The Examiner has rejected Claims 1, 4-18, 20, 27, and 29-30 under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (US Patent Number: 6,707,156) in view of Tanaka (US Patent Number: 6,100,589).

Group #1 – Claims 1, 4-16, 20, 27, and 29-30

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on appellant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir.1991).

With respect to the first element of the *prima facie* case of obviousness, the Examiner has stated that it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the integrated circuit of Suzuki et al. having the metal layer defined as mesh, such as taught by Tanaka in order to further improve the mechanical strength and to further enhance the effects for suppressing crack formation in the insulation interlayer so that it inherently prevents the damage to the active circuit and/or the at least one transistor during the bonding process. Appellant respectfully disagrees with this proposition, especially in view of the vast evidence to the contrary.

Specifically, it is noted that Tanaka merely addresses the problem of arranging bonding pads with high density, since a first electrode layer must have a large area in order to secure the bonding area, due to disconnection from bumps of aluminum wiring, etc. Note col. 1, lines 15-45 from Tanaka. Therefore, it is clear that Tanaka simply does not address the problem of bonding-related damage to the *active circuit*.

Still yet, it is noted that Suzuki does not even mention bonding, let alone the problem of bonding-related damage to the active circuit. Specifically, Suzuki merely teaches a technique for dealing with an increase of stress associated with increasing a height of a multilevel wiring layer structure. For example, Suzuki discloses that "if an interlayer insulating layer of SiOC is disposed between an organic insulating layer and a silicon oxide layer, the generation of stress and the like to be caused by a difference of a physical constant between the upper and lower level layers can be suppressed" (col. 6. lines 11-15). Thus, Suzuki simply does not even address the problem of bonding-related damage to the active circuit. To this end, neither prior art references even teaches the problem solved by appellant. See *Eibel Process Co. v Minnesota & Ontario Paper Co.*, 261 US 45 (1923).

In the Examiner's Answer mailed 11/30/2006, the Examiner has argued that "one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references." The Examiner has further argued that "[i]n fact, Suzuki discloses, as shown in Figure 1 and Col. 4, lines 58-64, that layer M11L is used as the pad, and an entirety of at least one of the transistors 13 is disposed directly below the pad," that "the pad is used as a connection to a wire or a bump," and that "the stress is occurred between the wiring layers and the crack could be formed in the insulating layers between the wiring layers."

The Examiner has also argued that "Tanaka discloses, as shown in Figures 1, 2A, 2B, 6A-9B, 19-22, and Col. 7, line 47-Col. 8, line 48, the meshed metal layer 200 that has the openings 130a-130i, and props composed of insulating interlayer are provided between the metal layers," and that "by forming the meshed metal layer, no cracks form in the insulating interlayer even if a load is applied during wire-bonding." The Examiner has therefore concluded that "it would have been obvious to combine the teaching of Tanaka into…Suzuki's invention to further improve the mechanical strength and to further enhance the effects for suppressing crack formation in the

insulating interlayer to that it inherently prevents the damage to the active circuit and/or the at least one transistor."

Appellant again respectfully disagrees.

Neither prior art references even teaches the specific problem solved (and claimed) by appellant

First, appellant takes issue with the Examiner's argument that combining the teachings of the prior art to suppress crack formation in the *insulating interlayer* would inherently prevent the damage to the *active circuit* and/or the at least one *transistor*. Such statement is baseless and without support in the prior art relied upon by the Examiner. To this end, appellant continues to assert that the Examiner fails to cite specific motivation *in the above references* to support the case for combining the same, for the purpose of preventing damage to the *active circuit* and/or the at least one *transistor*. *In re Regel*, 188 USPQ 132 (CCPA 1975).

It appears that the Examiner is attempting to rely on a different problem (e.g. *insulating interlayer* damage, etc.) identified in the prior art to support a motivation to combine the references for addressing a dissimilar purpose (e.g. preventing *active circuit* damage, etc.). To this end, appellant continues to contend that neither prior art references even teaches the problem solved by appellant. See *Eibel Process Co. v Minnesota & Ontario Paper Co.*, 261 US 45 (1923).

As evidence of such, appellant respectfully points out that Suzuki teaches that "[i]f insulating layers having very different physical constants are laminated, cracks or peeling is likely to be formed between the layers" (Col. 2, lines 50-52). Thus, clearly Suzuki relates to a problem of having multi-level wiring layers with different physical constants, which can cause cracks or peeling between the layers. Thus, Suzuki does not suggest a problem of *bonding-related* damage to an *active circuit*.

Still yet, appellant again respectfully asserts that Tanaka merely addresses the problem of arranging bonding pads with high density, since a first electrode layer must have a large area in

order to secure a bonding area, due to disconnection from bumps of aluminum wiring, etc. Therefore, it is clear that Tanaka also does not address the problem of *bonding-related* damage to the *active circuit*.

Again, neither of the prior art references even teaches the specific problem solved by appellant.

Lack of desirability of the combination in the prior art

In addition, Suzuki teaches "an insulating film having an intermediate physical constant [that] is inserted between two materials so that the generated stress may be relaxed" (Col. 8, lines 1-4) in order to prevent "insulating layers having very different physical constants [that] are laminated, [where] cracks or peeling is likely to be formed between the layers" (Col. 2, lines 50-52). Thus, Suzuki clearly teaches using an insulating film with an intermediate physical constant to eliminate the use of layers with different physical constants, thus preventing cracking and peeling between the layers.

Tanaka, on the other hand, teaches that "the insulating interlayers can be protected by the contiguous prop and thus crack formation is prevented" (Col. 2, lines 62-64) and that the "prop of the insulating interlayer film…[is] formed between the third electrode layer and the first electrode layer…[to] prevent cracks from forming in the insulating interlayers" (see Abstract). Tanaka discloses that such prop 140 "compris[es] the insulating interlayers [150, 160] [that are] formed between the first electrode layer 300 and the [third] electrode layer [100]" (Col. 6, lines 62-65 and Figure 1). As shown in Figure 1, the prop (which comprises the insulating interlayers 150, 160) extends from the first electrode layer 300 to the third electrode layer 100 via an opening 130e in the second electrode layer 200. Accordingly, Tanaka clearly teaches using a prop to prevent crack formation.

Thus, appellant respectfully asserts that the prior art does not suggest the desirability of the combination thereof or provide any motivation for such combination. In fact, as noted above, Suzuki solves the problem of cracking between *insulating layers* using an insulating film with an intermediate physical constant, whereas Tanaka solves the problem of cracking in the *insulating interlayers* using a prop. Thus, not only do the references address a different problem with

respect to appellant's specific claim language (e.g. cracking in *insulating layers* versus in an *active circuit*, etc.), they both do so by using completely different solutions. Therefore, there would have been no motivation to combine another solution, namely that of Tanaka, when one has already been presented, namely that of Suzuki, "to further improve the mechanical strength and to further enhance the effects for suppressing crack formation," as noted by the Examiner. Further, it is unclear whether the foregoing solutions are even compatible.

The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Although a prior art device "may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so." 916 F.2d at 682, 16 USPQ2d at 1432.).

Proposed combination of the prior art would change the principle of operation of the prior art invention being modified/References teach away from their combination

Furthermore, Suzuki teaches that "[i]f SiOC middle layers are used as the interlayer insulating layers for multilevel wiring layers excluding the etch stopper layer and hard mask layer, a change in the stress can be relaxed" and that "such relaxation of the stress may be ascribed to a gradual change in the dielectric constants of the lower, middle and upper interlayer insulating layers" (Col. 6, lines 31-33). Accordingly, Suzuki expressly teaches using SiOC, which is of a low dielectric constant, as the interlayer insulating layers in order to relax stress.

Thus, Suzuki clearly *teaches away* from adding any sort of metal mesh layer, as noted by the Examiner as being taught by Tanaka, since the addition of such metal mesh layer would impede the "gradual change in the dielectric constants" taught by Suzuki. It is improper to combine references where the references *teach away* from their combination. *In re Grasselli*, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983) Further, if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959)

Proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose

As further evidence of non-obviousness, appellant respectfully asserts that Suzuki expressly discloses, with respect to Figure 1, thereof, that the insulating interlayers are not directly connected. In particular, Suzuki discloses a hard mask layer (item 22) formed on the surface of the organic insulating layer (item 21), and a diffusion preventing and etch stopper layer (item 23) formed on the surface of the hard mask layer (item 22). Thus, the surface of each insulating layer in Suzuki is covered, such that the insulating interlayers are prevented from being directly connected. In addition, appellant respectfully points out that only the wiring layers (item M1L, etc.) are directly connected, which are buried in wiring trenches and via holes formed in the insulating interlayers, as shown in Figure 1 (Col. 4, lines 12-15).

Tanaka, on the other hand, discloses with respect to Figure 1 openings (items 130a-130i) through which the first insulating layer (item 160) and the second insulating layer (item 150) are connected/bonded to each other. In fact, the props in Tanaka, which are used to prevent cracks, are comprised of the connections between the insulating layers (Col. 6, lines 58-65). Thus, since Suzuki expressly discloses a disconnect between insulating interlayers, the props of Tanaka would be unable to be formed in the semiconductor device of Suzuki. If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose (as is the case here, as noted above), then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)

Therefore, for at least the reasons set forth hereinabove, the first element of the *prima facie* case of obviousness has simply not been met.

More importantly, with respect to the third element of the *prima facie* case of obviousness, the Examiner has relied on Figure 1 from Suzuki to make a prior art showing of appellant's claimed structure "wherein the [metal layer]... ensures that bonds are capable of being placed over the active circuit without damage thereto during a bonding process" (see this or similar, but not necessarily identical language in each of the independent claims).

Appellant respectfully disagrees with this assertion. First, as mentioned above, Suzuki does not even mention bonding, let alone the problem of bonding-related damage to the active circuit. Specifically, it is noted that Suzuki merely teaches a technique for dealing with an increase of stress associated with increasing a height of a multilevel wiring layer structure. For example, Suzuki discloses that "if an interlayer insulating layer of SiOC is disposed between an organic insulating layer and a silicon oxide layer, the generation of stress and the like to be caused by a difference of a physical constant between the upper and lower level layers can be suppressed" (col. 6, lines 11-15).

Such disclosure simply does not "ensure that bonds are capable of being placed over the active circuit," let alone "without damage thereto during a bonding process" (emphasis added), as claimed. It appears that the Examiner has admitted to not identifying the above emphasized claim language in the prior art. It also noted that the Examiner appears to rely on an inherency argument by arguing that the resultant combination *inherently* prevents the damage to the active circuit and/or the at least one transistor during the bonding process.

In response, appellant asserts that the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); *In re Oelrich*, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)

Appellant respectfully asserts that the claimed "mesh [which] ensures that bonds are capable of being placed over the active circuit without damage thereto during a bonding process" would be *unobvious* in view of the proposed prior art combination since only appellant teaches and claims the novel use of such meshed metal layer structure for the specific purpose of ensuring that bonds are capable of being placed over the active circuit without damage thereto during a bonding process, as claimed.

In summary, none of the references relied upon by the Examiner even suggest a mesh, as claimed by appellant, to ensure that bonds are capable of being placed over the active circuit without damage thereto during a bonding process.

In the Examiner's Answer mailed 11/30/2006, it appears the Examiner has failed to specifically respond to appellant's arguments above. In fact, the Examiner has merely argued that "one cannot show nonobviousness by attacking references individual where the rejections are based on combinations of references." The Examiner has also argued that, in Suzuki, "layer M11L is used as the pad" and that "the pad is used as a connection to a wire or a bump." In addition, the Examiner has argued that Tanaka discloses "the meshed metal layer 200."

These disclosures in the prior art, however, simply do not even suggest "ensur[ing] that bonds are capable of being placed over the active circuit without damage thereto during a bonding process," as appellant claims. For example, Suzuki only teaches that "[i]f insulating interlayers having very different physical constants are laminated, cracks or peeling is likely to be formed between the layers" (Col. 2, lines 50-52). However, appellant notes that, as described with respect to Figure 1 in Suzuki, the insulating interlayers (item 21, 24, etc.) are disposed above the semiconductor elements formed by the element separation region (item 12) (see Col. 3, line 61-Col. 4, line 27). Thus, preventing cracks *between insulating interlayers* which are disposed above semiconductor elements, as disclosed in Suzuki, does not even suggest the prevention of any sort of damage to the *active circuit*, as appellant claims, namely "ensur[ing] that bonds are capable of being placed over the active circuit without damage thereto during a bonding process" (emphasis added), as claimed.

In addition, Tanaka similarly discloses that the "props prevent cracks from forming in the insulating interlayers when a load is applied during wire-bonding" (Abstract-emphasis added) and that such "[c]racks will readily form in the hard insulating interlayers disposed between the conductive layers" (Col. 2, lines 60-62). Again, appellant respectfully asserts that cracks forming in the *insulating interlayers*, as in Tanaka, does not even suggest the prevention of any sort of damage to the *active circuit*, as appellant claims. Thus, neither the Suzuki nor Tanaka references teach appellant's specific claim language.

For these reasons, appellant respectfully asserts that the first and third elements of the *prima facie* case of obviousness have not been met, as noted above.

Group #2 – Claim 17

With respect to such claim, it is noted that the Examiner's rejection is still deficient. Specifically, the Examiner relies on Figures 7A and those shown below from Tanaka to meet appellant's claimed "wherein the interconnect vias include at least two spaced rows for each of the first portions."

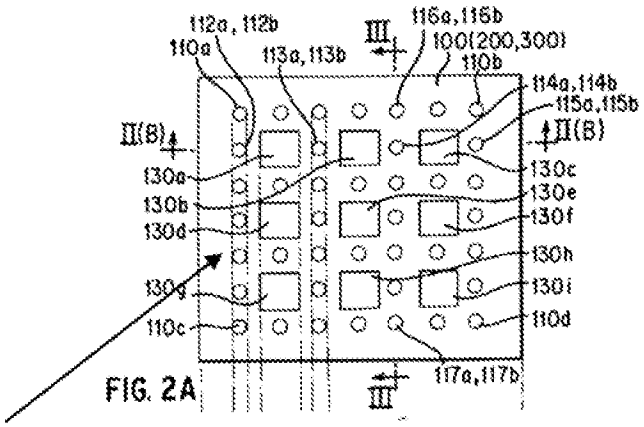

FIG. 2A

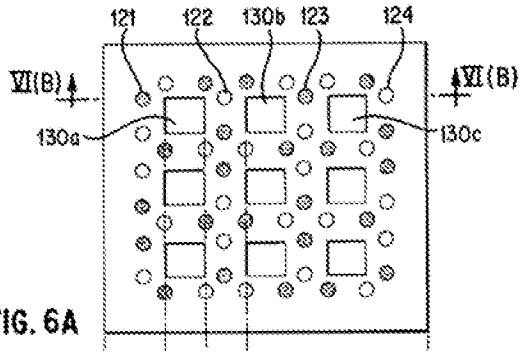

FIG. 6A

Specifically, the Examiner has argued that "interconnect vias (110a-c and 120a-c) include at least two spaced rows for each of the first portions." Appellant respectfully disagrees, as it appears that the Examiner has simply not taken into consideration the full weight of appellant's claim language. For example, appellant's claimed "first portions" are clearly defined as a plurality of substantially linear first portions which intersect a plurality of substantially linear second portions to define a matrix of openings (note intervening Claims 12-13). Thus, it is clear that appellant's claimed "first portions" each correlate with one of the rows annotated above by the arrow.

To this end, in no row of Tanaka is there any "at least two spaced rows" of "interconnect vias," as claimed. In fact, as noted in Figure 6A from Tanaka above, the rows thereof are not spaced (note the crowding and the interconnects positioned in the "second portions," which intersect the first portions, etc.).

In the Examiner's Answer mailed 11/30/2006, the Examiner has argued that "Tanaka discloses, as shown in Figures 9A and 9B, [that] the interconnect vias include at least two spaced rows (612a, 614a, 122a) for each of the first portions." Appellant respectfully disagrees. Figures 9A and 9B only show two rows of conductive layers (612a, 614a) on the outer periphery. However, around the openings (130e, 130d, etc.), only a single row of conductive layer is shown. Thus, Tanaka does not meet appellant's claimed technique "wherein the interconnect vias include at least two spaced rows for **each** of the first portions" (emphasis added), as claimed.

Appellant respectfully asserts that the first and third elements of the *prima facie* case of obviousness have not been met, as noted above.

Group #3 – Claim 18

With respect to such claim, it is noted that the Examiner's rejection is still deficient. Specifically, the Examiner relies on Figures 7A and those shown below from Tanaka to meet appellant's claimed technique "wherein a width of the first portions is enlarged to accommodate the at least two spaced rows for each of the first portions."

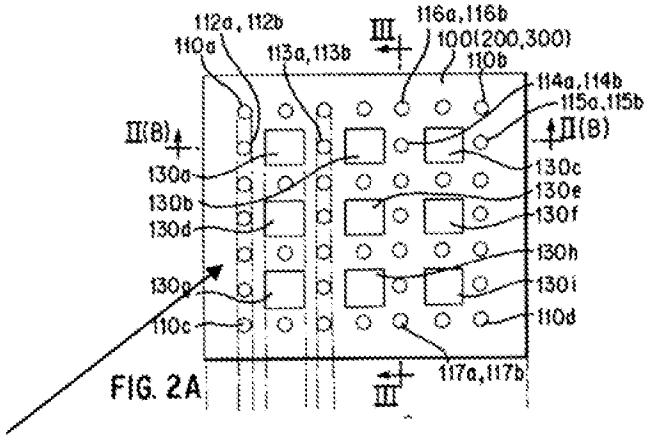

FIG. 2A

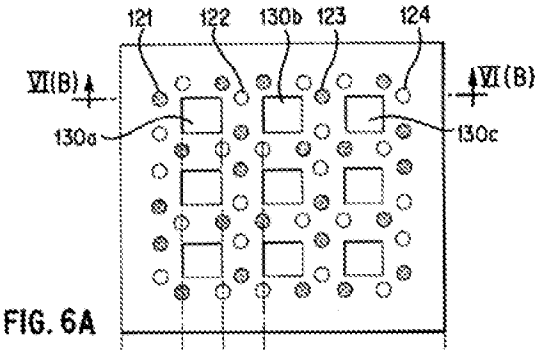

FIG. 6A

Specifically, the Examiner has argued that "interconnect vias (110a-c and 120a-c) include at least two spaced rows for each of the first portions." Appellant respectfully disagrees, as it appears that the Examiner has simply not taken into consideration the full weight of appellant's claim language. For example, appellant's claimed "first portions" are clearly defined as a plurality of substantially linear first portions which intersect a plurality of substantially linear second portions to define a matrix of openings (note intervening Claims 12-13). Thus, it is clear that appellant's claimed "first portions" each correlate with one of the rows annotated above by the arrow.

To this end, in no row of Tanaka is there any "at least two spaced rows" of "interconnect vias" formed thereon and "wherein a width of the first portions is enlarged to accommodate the at least two spaced rows for each of the first portions," as claimed. In fact, as noted in Figure 6A from Tanaka above, the rows thereof are not enlarged to accommodate any two spaced rows (note the crowding and the interconnects positioned in the "second portions," which intersect the first portions, etc.). Again, only appellant teaches and claims mesh first portions that have enlarged widths so that two spaced rows of vias are better accommodated.

In the Examiner's Answer mailed 11/30/2006, the Examiner has argued that "Tanaka discloses, as shown in Figures 9A and 9B, a width of the first portion is enlarged to accommodate the at least two spaced rows (612a, 614a, 122a) for each of the first portions." Appellant respectfully disagrees. Figures 9A and 9B only show two rows of conductive layers (612a, 614a) on the outer periphery. However, around the openings (130e, 130d, etc.), only a single row of conductive layer is shown. Thus, Tanaka does not meet appellant's claimed technique "wherein a width of the first portions is enlarged to accommodate the at least two spaced rows for **each** of the first portions" (emphasis added), as claimed.

Again, appellant respectfully asserts that the first and third elements of the *prima facie* case of obviousness have not been met, as noted above.

Issue # 3:

The Examiner has rejected Claims 2, and 21 under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (US Patent Number: 6,707,156) in view of Tanaka (US Patent Number: 6,100,589), and in further view of Applicant's Admitted Prior Art of Figures 1 and 2.

Group #1 – Claim 2

Appellant respectfully asserts that such claims are not met by the prior art for the reasons argued with respect to Issue #2, Group #1.

Again, appellant respectfully asserts that the first and third elements of the *prima facie* case of obviousness have not been met, as noted above.

Group #2 – Claim 21

With respect to appellant's claimed "meshed interconnect metal layer disposed, at least partially, above the I/O bus of the active circuit," the Examiner has argued that "Applicant's Admitted Prior Art of Figures 1-2 disclose … a plurality of … metal layers (M1-M4), at least partially, under the active circuit." Whether this is true or not, the Examiner has still not considered the full weight of appellant's claims. Note Figure 2 below.

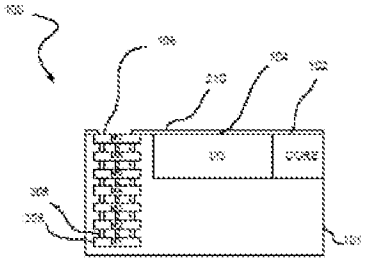

FIG. 2
(Prior Art)

The Examiner has argued that the foregoing figure discloses an active circuit including an input/output bus and metal layers, at least partially, under the active circuit.

However, the Examiner's art and arguments simply do not address appellant's claimed "meshed interconnect metal layer disposed, at least partially, above the I/O bus of the active circuit," as claimed.

In the Examiner's Answer mailed 11/30/2006, the Examiner has argued that "Suzuki discloses, as shown in Figure 1 and Col. 4, lines 58-64...the integrated circuit comprising an active circuit (13), a metal layer (M1L-M10L) disposed, at least partially, above the active circuit, a pad (M11L), and an entirety of at least one of the transistors (13) is disposed directly below the pad" and that "Tanaka discloses...[that] the metal layer 200 is meshed."

Appellant respectfully disagrees. For example, Suzuki only teaches wiring layers (M1L-M11L) located above an element separation region (12) that is formed and a number of semiconductor elements such as MOS transistors are formed. However, simply disclose wiring layers disposed over an element separation region, as in Suzuki, does not specifically teach "a...metal layer disposed, at least partially, above the I/O bus of the active circuit" as opposed to other portions of the active circuit (emphasis added), as appellant claims. In addition, Prior Art Figures 1 and 2 of appellant's specification only generally show an active circuit that includes an I/O bus and a core, but do not specifically teach "a...metal layer disposed, at least partially, above the I/O bus" (emphasis added), as claimed.

Still yet, Tanaka only generally teaches the meshed metal layer noted by the Examiner as being included in the bonding pad (Col. 6, lines 20-29 and 58-59), but not specifically "a meshed interconnect metal layer disposed, at least partially, above the I/O bus of the active circuit" (emphasis added), as specifically claimed by appellant.

Yet again, appellant respectfully asserts that the first and third elements of the *prima facie* case of obviousness have not been met, as noted above.

In view of the remarks set forth hereinabove, all of the independent claims are deemed allowable, along with any claims depending therefrom.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 971-2573. For payment of any additional fees due in connection with the filing of this paper, the Commissioner is authorized to charge such fees to Deposit Account No. 50-1351 (Order No. NVIDP234).

Respectfully submitted,

By: /KEVINZILKA/ Date: January 30, 2007

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